Official Amendment
Serial No: 09/943,078
Attorney Docket MIO 0083 PA

REMARKS

In the present application, claims 1-16 and 39 are pending. Claims 12 and 13 are cancelled herein. Further, non-elected claims 29-38 and 40-44 are canceled herein. Claims 1 and 39 are amended herein. The amendment to claim 1 is not made for reasons of patentability. Rather, the amendment herein is provided for contextual purposes, to add clarity to the claim, and to make explicit that which was already implicit in the claim. Finally, new claims 45-49 are added herein.

In The Drawings

The drawings were objected to under 37 C.F.R. §1.83(a). The Examiner asserts that the gate area and local interconnect area are not shown in the same trench as claimed in claims 1 and 39. The applicant respectfully traverses this objection. Referring to Fig. 16, one example is given where both local interconnect areas and gate areas are illustrated in the same damascene trench. As shown, a first damascene trench, identified as strip 268 includes gate 214 and 222. The gates 214 and 222 are constructed by building damascene gate structures. The strip 268 (damascene trench) further includes first and second contacts 270 and 272 constructed as damascene local interconnect structures. See page 15, lines 15-27. The applicant asserts that, for all of the above reasons, the application is in compliance with 37 C.F.R. §1.83 for purposes of claims 1 and 39.

The applicant also respectfully traverses the Examiner's objection to claim 4 for not explicitly showing the steps in the formation of the isolation region. The applicant agrees with the Examiner that some steps claimed in claim 4 are not shown with specificity. However, 37 C.F.R. §1.83(a) states that conventional features disclosed in the description and claims should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a lab led rectangular box), where their detailed

illustration is not essential for a proper understanding of the invention. The present application makes it clear that the manner in which the isolation trench is formed is not important to practicing the present invention. "The isolation trench 14 defines an isolation region, and is formed using any available techniques including for example, shallow trench isolation (STI) methods". Specification page 7, lines 12-14.

STI trench formation is not essential to an understanding of the present invention. Therefore the applicant did not show each step claimed in claim 4 with detailed specificity. Rather, the applicant illustrates the formed STI region in Figs. 1-13. Formation of the isolation regions as claimed is further explicitly described in the Specification on page 7 lines 25-29; page 8, lines 1-5. Moreover, trench formation is shown by a rectangular box 152 in the flow chart of Fig. 14. The applicant asserts that, for all of the above reasons, the application is in compliance with 37 C.F.R. §1.83 for purposes of claim 4.

The drawings were objected to for not showing a silicide layer between the base substrate and polysilicon as claimed in claim 12. Claim 12 is cancelled herein. The drawings were also objected to for not explicitly illustrating the steps disclosed in claim 13. Claim 13 has been cancelled herein.

OBJECTION TO THE SPECIFICATION

The Examiner objects to the disclosure on page 13, lines 1 and 2. The specification is amended herein to make clear cobalt is not a silicide. Rather, the layer of cobalt is deposited and a subsequent anneal process is performed such that $CoSi_x$ is formed on the polysilicon conductive layer and active areas. Accordingly, the applicant requests that the Examiner withdraw the objection to the specification.

The Examiner further objects to the specification because the process steps of claim 13 is not in the specification. Claim 13 has been cancelled herein. Accordingly, the applicant requests that the Examiner withdraw the objection to the specification.

35 U.S.C. §112

Claims 1-16 and 39 were rejected under 35 U.S.C. §112 first paragraph. The Examiner asserts that the specification is not enabling for forming a gate structure and an interconnect structure in the same trench. The applicant respectfully traverses this rejection. The application makes clear that each damascene trench can actually include any combination of gates and local interconnects. The Figs. 4-13 show the formation of both a gate and local interconnect. For purposes of clarity, a gate is formed in the damascene trench 44 (on the left hand side of the Figs.) and a local interconnect is shown in the damascene trench 46 (on the right hand side of the Figs). However, the specification makes clear that the damascene trenches are not limited to either a gate of an interconnect.

> "Further, any combination of gates and local interconnects can be formed within *each* of the gate/local interconnect damascene trenches 44, 46 as explained more fully herein" (emphasis added) Specification page 9, lines 10-12.

Also, one specific example is shown of using the techniques taught in the present invention to build an SRAM memory device as shown with reference to Figs. 15-16. As shown in Fig. 16, first and second strips 268, 274 (as well as word line 255) form conductive interconnects and may be fabricated as damascene trenches as discussed with reference to Figs. 1-13. Specification Page 15, lines 11-17.

The gates 214 and 222 are constructed as part of the first strip (damascene trench) 268 by building damascene gate structures. The first contact and second contact 270, 272 are constructed as part of the first strip 268 by building damascene local interconnect structures. Likewise, the gates 224, 232 are constructed as part of the second strip (damascene trench) by building damascene gate structures. The third and fourth contacts 276, 278 are constructed as part of the second strip (damascene trench) by building damascene local interconnect structures. Specification Page 15, lines19-30.

The specification states that any combination of gates and local interconnects may be formed in a given damascene trench. Moreover, one exemplary structure discussed with reference to Figs. 15-16 illustrates two damascene trenches, each damascene trench having two local interconnect contacts and two gates formed therein. Accordingly, the applicant asserts that the specification is enabling to one of ordinary skill in the art, for the teaching that a gate and local interconnect can be constructed in the same damascene trench.

35 U.S.C. §102

Claims 1-3, 5, 6 and 10 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,261,905 B1 (Chen et al.). According to the M.P.E.P. §706.02, in order to be anticipating under §102, the reference must teach every aspect of the claimed invention. *Carella v. Starlight Archery and Pro Line Co.*, 804 F.2d 135, 138, 231 U.S.P.Q. 644, 646 (Fed. Cir. 1986).

With respect to claim 1 as amended herein, Chen fails to teach forming a damascene trench in a first dielectric layer, the damascene trench having a gate area and a local interconnect area and removing the first dielectric layer to define a damascene gate structure and a damascene local interconnect structure, the damascene local interconnect structure forming a connection to the base substrate.

Chen teaches a method of forming stacking gate structures for flash memory devices. Shallow trench isolation regions are formed in the substrate. Next, a tunnel oxide layer is formed over the substrate. A nitride layer is formed over the substrate including the STI layers. The nitride layer is patterned and etched to form damascene trench regions. A first polysilicon layer is conformally deposited over the base substrate and oxide layers, and is then patterned and etched to define delineations transverse to the damascene trenches. Etching of the first polysilicon layer to define the delineations takes place over the shallow trench isolation regions (Col. 7, lines 60-67). An inter-gate, capacitive dielectric is conformally formed over the first polysilicon and a second polysilicon is formed over the capacitive dielectric.

Chen does not teach or even mention local interconnects to the base substrate as claimed. As the specification describes, and the figures support, the only structures formed in the damascene trenches are stacked gate structures for flash memory devices. The first polysilicon layer is a floating gate electrode and not a local interconnect to the base substrate. Even the second polysilicon fails to form a local interconnection to the base substrate. As is best seen in Fig. 4d, the second polysilicon is spaced from the base substrate by the first polysilicon layer and the gate oxide. Even in the delineations, the second polysilicon is spaced from the base substrate by the inter-gate dielectric and gate oxide. Further, the specification makes it clear that the delineations are *only* formed over the STI regions (Col. 7, lines 60-67). (This is to prevent damage to the active areas) and thus deliberately avoids the active areas of the base substrate.

Chen does not teach every element of the claimed invention as required by the M.P.E.P. §706.02 as set out above. Accordingly, the applicant requests that the Examiner withdraw the rejection of claim 1 and the claims that depend therefrom including claims 2-3, 5, 6 and 10 under 35 U.S.C. §102( ).

35 U.S.C. §103(a)

Claims 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Chen in view of the article Silicon Processing For The VLSI Era, Volume 2 – Process Integration by Lattice Press (hereinafter "Wolf"). The Examiner asserts that Chen teaches all of the limitations of the claimed invention except for the details in the formation of the isolation trenches. According to the M.P.E.P. §2143.03, to establish a *prima facie* case of obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

As pointed out above, Chen fails to teach forming a damascene trench in a first dielectric layer, the damascene trench having a gate area and a local interconnect area and removing the first dielectric layer to define a damascene gate structure and a damascene local interconnect structure, the damascene local interconnect structure forming a connection to the base substrate.

Wolf does not teach or suggest the formation of damascene trenches at all. Further, Wolf does not teach or suggest the formation of interconnects. Accordingly, the applicant requests that the Examiner withdraw the rejection of claim 4 under 35 U.S.C. §103.

Claims 7, 11 and 14-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Chen in view of U.S. Patent No. 6,287,926 (hereinafter "Hu").

As pointed out above, Chen fails to teach forming a damascene trench in a first dielectric layer, the damascene trench having a gate area and a local interconnect area and removing the first dielectric layer to define a damascene gate structure and a

damascene local interconnect structure, the damascene local interconnect structure forming a connection to the base substrate.

Hu teaches the formation of a damascene trench where the trench extends below the surface of the base substrate by the small amount. A thinox region is formed on the channel floor of the trench. Further, lightly doped regions and a channel stop area, and a pocket implant are formed. Spacers are formed on the trench walls, then the thinox is removed leaving the oxide in the extreme corners of the channel floor. After completion of the gate, the resulting structure is a device with an elevated source/drain region and a gate with a self-aligned channel implant (Col. 9, lines 47-59). As second embodiment further includes a silicided layer over the polysilicon gate electrode and disposable spacers that allow the formation of the lightly doped drain (LDD) regions of the source/drain areas (Col. 10, lines 8-21). Yet a third embodiment over etches the spacers such that the silicided layer formed over the polysilicon gate electrode can extend the width of the polysilicon plus the width of the spacers (Col. 10, lines 61-67).

However, Hu fails to teach forming a damascene trench in a first dielectric layer, the damascene trench having a gate area and a local interconnect area and removing the first dielectric layer to define a damascene gate structure and a damascene local interconnect structure, the damascene local interconnect structure forming a connection to the base substrate. In fact, the applicant can find no teaching in Hu as to the formation of an interconnect to the base substrate and the formation of a gate structure. Rather, all three embodiments are directed to the formation of gate electrodes in a damascene trench. Accordingly, the applicant requests that the Examiner withdraw the rejection of claims 7, 11, and 14-16 and the claims that depend therefrom, under 35 U.S.C. §103(a).

Official Amendment
Serial No: 09/943,078
Attorney Docket MIO 0083 PA

Allowable Subject Matter

The Examiner indicated that claims 8, 9, 12, 13 and 39 would be allowable if rewritten in independent form. The applicant would like to thank the Examiner for the indication of allowable subject matter. The above claims are not rewritten in independent form herein because the applicant believes that claim 1, as amended herein, defines over the art of record.

New Claims

The applicant believes that the new claims added herein are patentable over the art of record. Specifically, new claims 45-49 are added herein. Each new claim is dependent upon claim 1, which the applicant believes to be patentable over the art of record as amended herein.

CONCLUSION

For all of the above reasons, the applicant respectfully submits that the above claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
KILLWORTH, GOTTMAN, HAGAN
& SCHAEFF, LLP

By _____
Thomas E. Lees Reg. No. 46,867

One Dayton Centre
One South Main Street, Suite 500
Dayton, Ohio 45402-2023
(937) 223-2050
Facsimile: (937) 223-0724
E-mail: leest@kghs.com

Official Amendment
Serial No: 09/943,078
Attorney Docket MIO 0083 PA

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the paragraph starting on page 12, line 29 with the following:

Further, where the conductive layer comprises a polysilicon, an optional silicide layer may be desirable. Referring to Fig. 12B, after the formation of the spacers 102 and further doping is performed to define the doped source/drain regions 96, the silicide layer 71~~, cobalt for example,~~ is deposited over the structure 10. For example, a~~A~~fter~~-~~ cobalt is deposited and a subsequent anneal process is performed, $CoSi_x$ is formed on the polysilicon conductive layer 70 and active areas, including the doped source/drain regions 96. The silicide layer 71 serves to lower the resistance of the polysilicon conductive layer 70. Subsequent chemical etches remove the un-reacted film (cobalt) from the spacers 102 and other dielectrics.

IN THE CLAIMS

1. (Amended) A method of fabricating a semiconductor device comprising:

forming a first dielectric layer over a base substrate;

forming a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area;

forming a gate oxide layer on said base substrate within said gate area of said damascene trench;

filling said damascene trench with a conductive material; and,

removing said first dielectric layer to define a damascene gate structure and a damascene local interconnect structure, said damascene local interconnect structure forming a connection to said base substrate.

39. (Amended) A method of fabricating a semiconductor device comprising:

forming an isolation trench in a base substrate

forming a first dielectric layer over said base substrate;

forming a first patterned mask over said first dielectric layer;

etching through said first dielectric layer to said base substrate in areas defined by said first patterned mask to define a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area; and positioned such that at least a portion of said damascene trench at least partially overlies said isolation trench;

stripping said first patterned mask from said first dielectric layer;

growing an oxide layer on said base substrate, said oxide layer within said gate area of said damascene trench defining a gate oxide layer;

forming a second patterned mask over said semiconductor device, said second patterned mask arranged to expose at least a portion of said oxide layer within said local interconnect area;

etching away the exposed portion of said oxide layer within said damascene trench;

providing at least one contact implant within said base substrate through said damascene trench;

stripping said second patterned mask from said semiconductor device;

depositing a conductive layer comprising a conductive material over said device such that said conductive layer fills said damascene trench;

planarizing said conductive layer down to the surface of said dielectric layer;

removing said first dielectric layer to define a damascene gate structure and a damascene local interconnect structure;

forming lightly doped drain regions in said base substrate adjacent to said damascene gate structure and said damascene local interconnect structure;

depositing a spacer layer over said device;

anisotropically etching said spacer layer such that spacers are formed over the portions of said base substrate where said lightly doped drain regions are formed; and,

forming doped source/drain regions in said base substrate after forming said spacers such that said base substrate is doped more deeply into said base substrate adjacent to said spacers than into said base substrate underneath said spacers.